User's Guide – ES100 Application Development Kit

DESCRIPTION

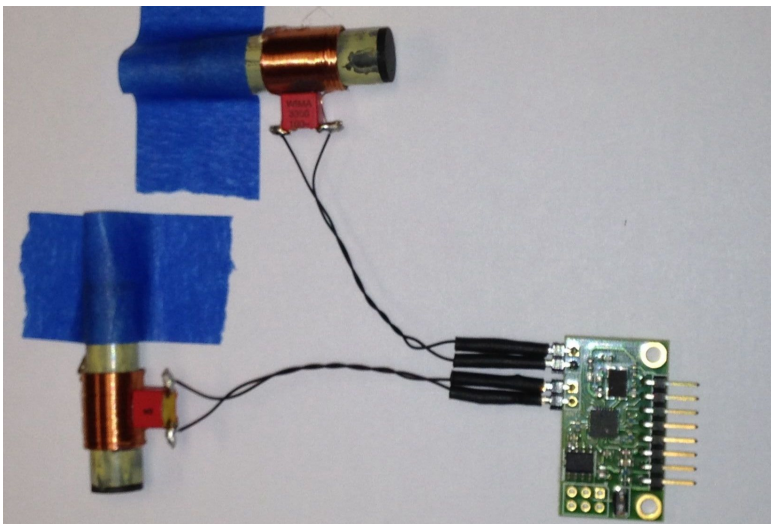
The ES100 Application Development Kit (ADK) is a dual-antenna receiver module for the phase-modulated time-code signal that is broadcast from the WWVB radio station in Ft. Collins, CO. Details about the station and the broadcast may be found at: http://www.nist.gov/pml/div688/grp40/wwvb.cfm.

The dual antenna configuration of this module greatly improves its ability to receive the WWVB signal. If one antenna is oriented such that the direction of the signal is at its null, the other one, positioned perpendicular to it, will be oriented for maximum signal strength (broadside towards direction of the signal). Furthermore, if the module is located near a source of interference, one antenna may be less susceptible to its emissions than the other.

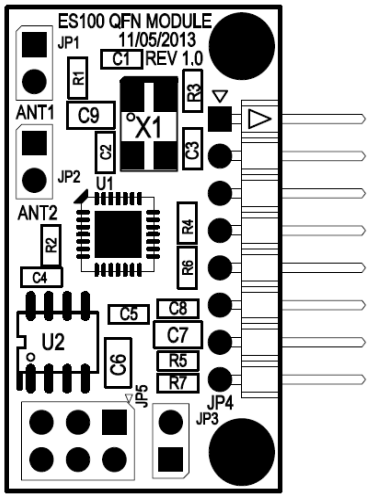
Refer to the ES100 Data Sheet for information on the register map and serial interface.

QUICK START GUIDE

1. Connect antennas to the ES100 module. Position them so they are perpendicular to each other and parallel to the floor.
2. Connect pin 1 to a DC voltage source (2v – 3.6V) and connect pin 6 to the ground return. (It is a good idea to twist this wire pair.)
3. Connect IRQ-, SCL, SDA, and EN to the host Microcontroller.
4. Start the reception by writing to the ES100 Control 0 register. (Refer to page 17 of the ES100 data sheet for valid Control 0 register write values.)
5. Respond to interrupts as they occur. (The falling-edge of the IRQ- signal is timed to the received WWVB second boundary, as documented in Figure 4 in the data sheet.)



COMPONENT LAYOUT AND PIN ASSIGNMENT

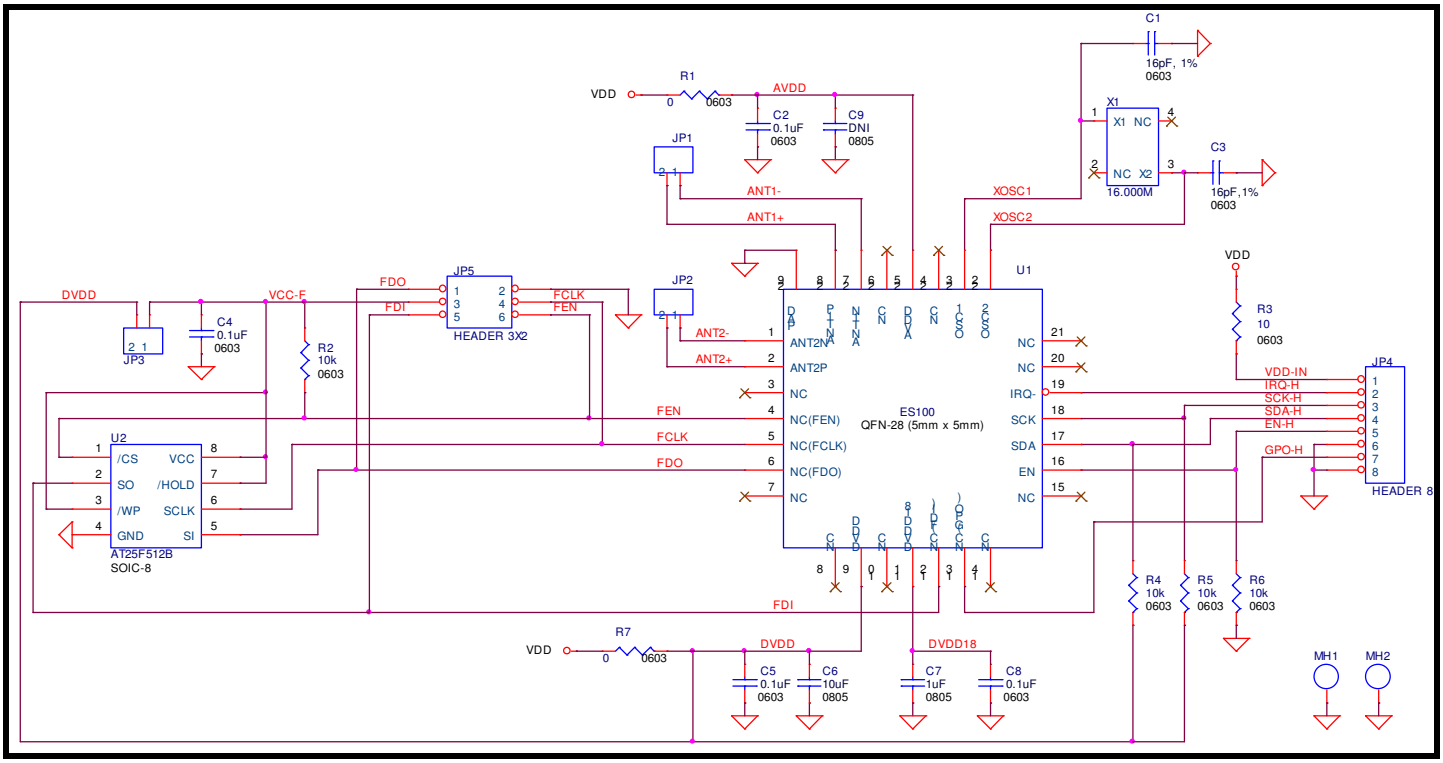


Pin 1: VDD (2 V - 3.6 V)
Pin 2: $\overline{\text{IRQ}}$
Pin 3: SCK
Pin 4: SDA
Pin 5: EN
Pin 6: GND
Pin 7: GPO
Pin 8: GND

SIGNAL DESCRIPTION

Pin Name	Description	Type	Input/ Output	Pin No.
VDD	**Power Supply** 2.0V to 3.6V	power	I	1
$\overline{\text{IRQ}}$	**Interrupt Request** Falling edge indicates an interrupt request.	digital	O	2
SCK	**Serial Interface Clock** On-board, 10kΩ pull-up to VDD.	digital	I	3
SDA	**Serial Interface Data** On-board, 10kΩ pull-up to VDD.	digital	I/O	4
EN	**Enable** When low, the ES100 powers down all circuitry. When high, the device is operational. Must be held low until VDD has stabilized.	digital	I	5
GND	**Ground**	power	I	6
GPO	**Reserved**	digital	O	7
GND	**Ground**	power	I	8

SCHEMATIC



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