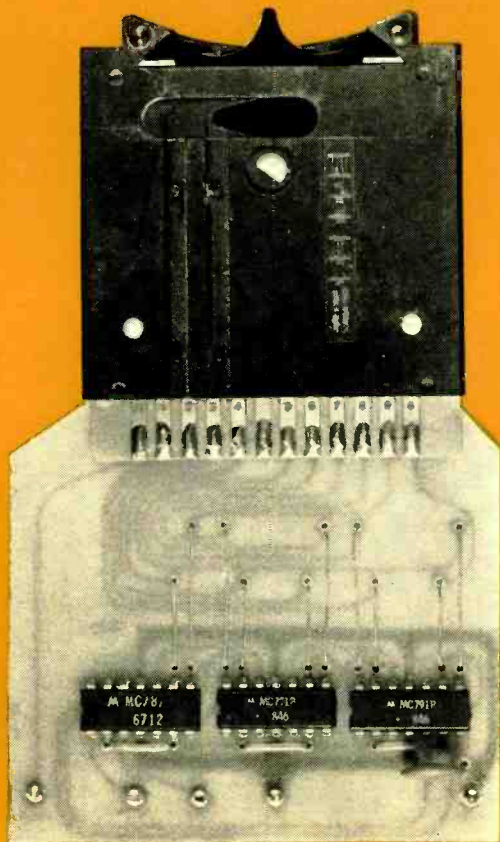


# Predetermining Decimal Counter

By DONALD E. LANCASTER

*A unique, inexpensive decade counter that can be cascaded to divide by any number from 1-99, 1-999, etc. It uses an ordinary single-pole, 10-position selector switch in place of usual gates and/or decoding circuits.*



Prototype version of RTL predetermining decimal counter mounted on the back of thumbwheel switch.

TODAY'S digital circuit designer has a wide choice of decimal counting techniques available. Many of these general-purpose techniques have been described in past issues of *ELECTRONICS WORLD* ("IC Decimal Counting Techniques," September, 1968, "IC Frequency Dividers & Counters," December, 1968 and January, 1969) and are also covered in the author's book, "RTL Cookbook," published by *Howard W. Sams & Co., Inc.* Described here is a special-purpose decimal counter with several unique features.

This counter is simple and low in cost. It takes three IC's and one single-pole, 10-position selector switch, and can be built for as little as \$8.50 per decade. The technique works with any IC family; RTL (Resistor-Transistor Logic) is used in the prototype circuits and kits of both TTL (Transistor-Transistor Logic) and RTL are available.

What makes the counter unique is that you can force it to count to any selected number from 0 to 9 and then repeat or stop. This is done using no gates, no decoding, and only an ordinary single-pole, 10-position selector switch (either rotary, thumbwheel, or push-button). Even more unusual is the fact that you can directly cascade counter stages without any additional circuitry to form 0-99, 0-999, 0-9999, etc. predetermining counters that can be directly preset to the desired decimal number. Note that if we attempted to cascade an ordinary divide-by-three with a divide-by-two and a divide-by-one, we would get only a divide-by-six output. This circuit will divide by 321 when three such stages are preset and cascaded.

The circuit is called a *phase-shift ring* and is a simple and new variation on a popular decimal counter called a walking-ring counter, also known as a Johnson counter, switchtail ring, etc.

On the debit side, to get the required cascade arrangement, this counter counts in a very odd-ball manner; it cannot drive a readout or provide an electrical output on anything but the selected count. It's also necessary to throw in a "free" count at the beginning of each use—but we'll shortly see that this is very easy to do.

## Applications

A counter of this type can be used anywhere you want a set of knobs or a series of thumbwheels that you can set to some decimal number and, in turn, get out either that many events or pulses, a signal that lasts for that many counts, or a ratio between either pulses or frequencies of the preset number. Some typical applications are in predetermining process controls that stop on a preselected count; digital photo timers that count the power line for excellent long-term accuracy; lab scalars for dividing down input frequencies of nuclear pulses and other instrumentation signals; frequency synthesizers, either as v.f.o. replacements, musical-tuning aids, or ultra-stable audio oscillators; and computers and calculators either for keyboard entry or pulse-rate computation circuits.

## How It Works

The well-known walking-ring decade counter is shown in Fig. 1. This popular circuit uses five JK flip-flops (boxes) to perform decimal counting.

Each flip-flop is a storage device and has a Q and a  $\bar{Q}$  output. These outputs are always *complementary* in that if one is grounded the other is always positive and *vice versa*. In this circuit, whenever the input to the flip-flop's "T" terminal abruptly goes from "+" to ground, whatever *was* on the "S" (Set) and "C" (Clear) terminals gets passed to its corresponding Q and  $\bar{Q}$  terminals. A built-in time delay (90 nanoseconds for RTL) assures that the stored information is passed along *only* one stage at a time. Thus, each flip-flop, under command, passes the signals on its outputs one stage to the right.

To make a counter, we add a *buffer* (B triangle) between the count input and the Toggle terminals (Fig. 1). This gives

us enough power to drive five Toggle inputs synchronously without requiring an excessively strong input signal. The buffer also inverts the input signal, so that any time the Count input goes positive, a negative transition from "+" to ground is sent to each Toggle input, and each flip-flop passes its input to the flip-flop on its right.

We also have an inverter and a buffer on the Reset ( $C_D$ ) input and whenever the Reset input goes positive, all of the flip-flops immediately go into the state with the Q outputs grounded and the Q outputs positive.

Suppose we reset our counter and call a positive terminal condition a "0" and a grounded condition a "1." Looking at the Q outputs, our counter will be in a state of 11111. With the receipt of one Count input pulse each "1" (Q output) will pass to the flip-flop on the right. However, the rightmost "1" is effectively complemented (becomes a "0") when passed to the leftmost flip-flop, giving us 01111. This occurs because the "0" (Q) output of the rightmost flip-flop is present on the S input of the leftmost flip-flop when the count input pulse arrives. As shown in the timing diagram of Fig. 1, additional Count pulses sequentially advance the counter to 00111, 00011, 00001, 00000, 10000, 11000, 11100, 11110, 11111, and then begins to repeat itself. There are ten different states, so this is a counter that repeats itself every ten counts.

If we were building an ordinary decimal counter, we probably would decode each state with a two-input gate, and proceed to drive a readout of some sort. We would probably also add a protection circuit to guarantee that the counter does not deviate from the above sequence.

### The Significant Difference

The key to the predetermining phase-shift counter lies in how we use the basic walking-ring circuit. Look at the waveforms of Fig. 1; each output has one, and only one, positive transition per 10 counts, and there is a different positive transition available at some terminal for each of the ten counts. We simply use a single-pole, ten-position selector switch (Fig. 2) to route the selected positive output transition to act as the Carry input for the next stage. Thus, instead of carrying on a zero after count nine, we select a carry that corresponds to the selected positive transition.

Suppose we cascade several decades and reset them to zero. The first time each decade goes around, it counts by the selected number; on all succeeding counts, it divides by ten. Whenever we reach the desired total count, a positive Carry output is produced, which can stop the process, turn off the timer, or can be used to recycle the counter for continuous operation.

### Problem Zeros

The above scheme works fine on most counts, but zeros can present a problem. If a counter decade is set to zero, a positive transition may not be obtained until the counter goes once around, throwing off the total by at least ten counts. Clearly, something has to be done to the basic counting idea to get the counter decade to work for all settings.

There are several possible solutions: One is to add an external gate to the first stage and re-define the first stage switch positions. While this works, it makes the first decade slightly different from the others, leading to two different kinds of PC layouts and possible later mixups.

Another reasonable alternative is called the "Add One" technique. This is the one used here. To get the counter to work properly for any count, we reset to 9999—instead of 0000. We also toss in a "free" count at the beginning to make up the difference. The free count is easy to pick up—we'll see just how in a minute. With the free count, even if we have a counter set to zero, we'll still get the needed carries at the right time, and the circuit will work for all counts.

The practical counter is shown in logic-diagram form in Fig. 2 and a schematic of the RTL prototype version is shown

in Fig. 3. (A kit of all parts shown in Fig. 3, less switch S1, but including etched and drilled PC board can be obtained from Southwest Technical Products, Box 16297, San Antonio, Texas 78216 for \$8.50 per decade, postpaid. TTL version is available at \$10.50 per decade, postpaid.) The prototype unit is shown in the lead photograph. Prototype and kit units can be mounted on the back of an Intermarket thumbwheel switch, Type S110ND (Allied Radio #56 D 6964).

### An Example

The counter counts in a very unorthodox manner, but gets

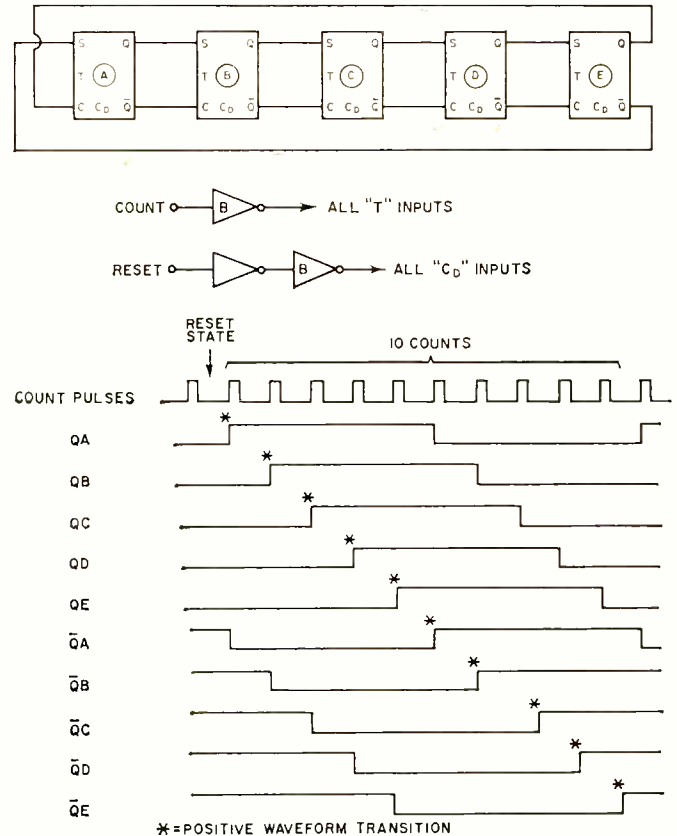
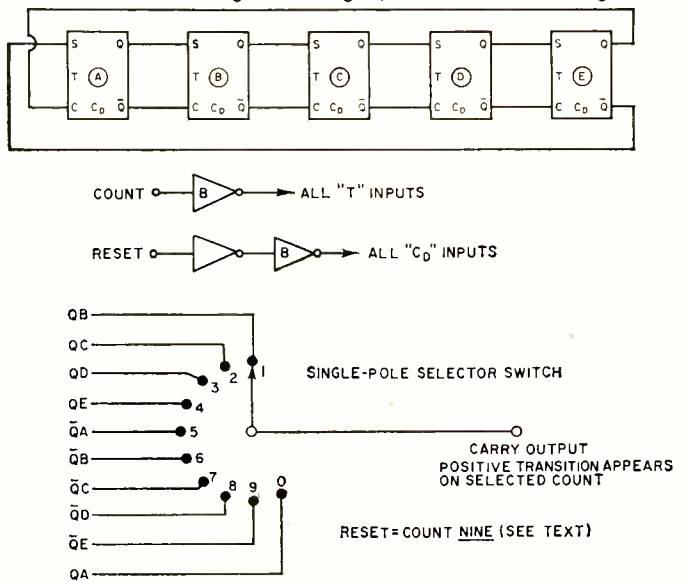


Fig. 1. Logic diagram and timing chart of walking-ring decade counter. Data present on "Q" outputs of each JK FF, except for rightmost FF, as noted, is passed on to FF on its right when the count input pulse is fed simultaneously to all "T" inputs.

Fig. 2. Walking-ring decade and single-pole, ten-position selector switch used to develop the predetermining counter. The switch is set to route one of the positive output transitions, as shown in the timing chart of Fig. 1, to the next counter stage.



NOTE: COUNTER RESETS TO 9. ADD "FREE" COUNT AT BEGINNING OF SEQUENCE. (SEE TEXT)

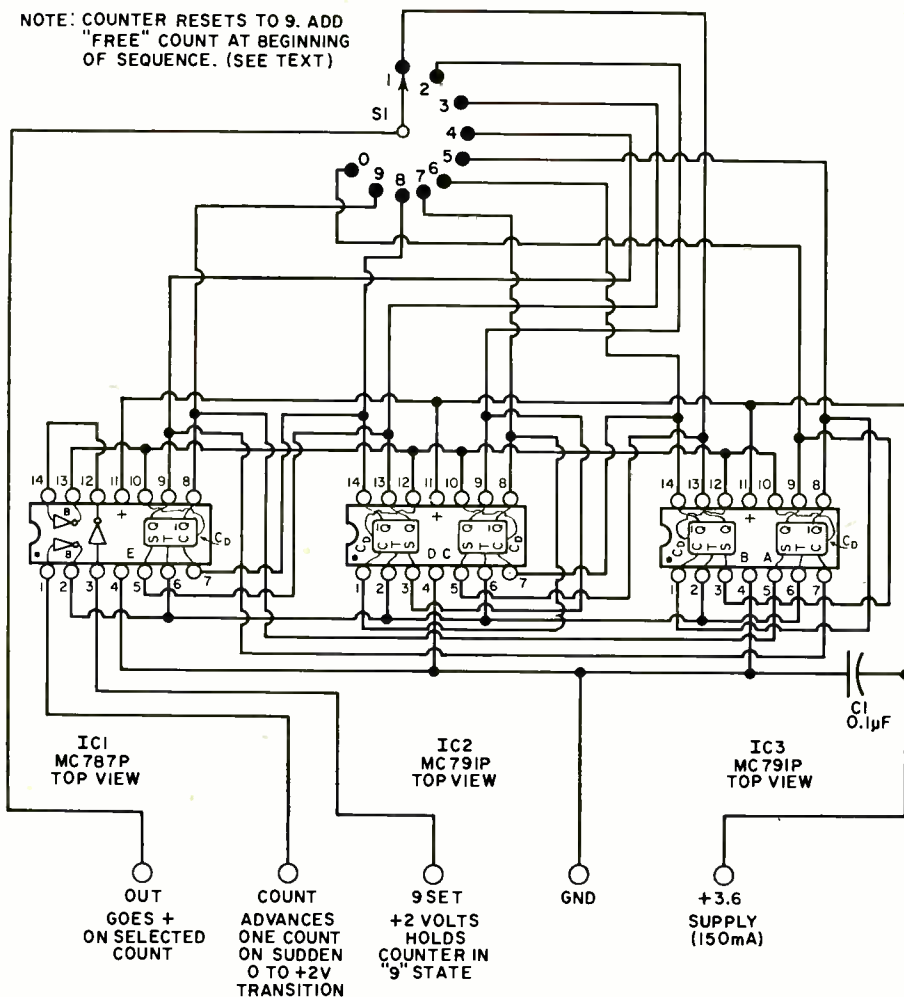


Fig. 3. Schematic diagram of the RTL prototype version of the predetermining decade counter using a rotary, 10-position selector switch.

the job done with a minimum number of parts and at minimum cost. Let's look at a typical count situation that will help explain the operation of the predetermining counter.

Suppose we cascade two stages that are set to give us an output after seventeen counts.

The fastest counter will produce a positive carry on count "7." The slower one will produce a carry and a useful output signal on count "1."

We reset our counters to 99 and throw in a free count. This gives us a 90. No carry is produced because the fast counter is set to carry on "7," not on "0." Now we start counting: 91, 92, 93, 94, 95, 96, 07. Here a carry was produced, because we carry on count "7" with the faster counter. We continue: 08, 09, 00, 01, 02, 03, 04, 05, 06, 17 and get a positive output transition on the last count. Going back to count all the numbers after the free count, you'll find it took just exactly the preset 17 counts to get an output. (Note the 00 condition pops up in the middle of the count instead of at the beginning, guaranteeing a positive pulse, if needed, at the right time.)

### Some Precautions

As with an electronic counter, we have to obey some rules to get it to work properly. With RTL, we have to have a well bypassed power supply with good grounds and be within 10% of 3.6 volts. About 150 mA is needed per decade, or around an amp or so for a complete six-decade chain. The operating frequency of the RTL version approaches 8 MHz, but the control and recycle circuitry slows things down considerably. Without careful design techniques on the control and reset circuitry, a 1-MHz limit is practical for the circuit; more can be obtained by careful consideration of

the control and recycle timing pulses.

All input counts must be made bounceless and noise-free, going positive once and only once per desired count with a rise-time of 1 microsecond or faster. We can cascade decades directly by connecting the Carry output of the first to the Count input of the next one. We can only let the counter run once, and then reset it to 9999 . . . , throw in a free count, and start over again. It is also wise to *hold* the counter in the 999 . . . state between uses. This eliminates any chance of starting off on the wrong foot.

The output consists of a positive-going signal on the selected count, whose leading edge may drive up to two logic gates for outside control. Any "Add One" circuit added to the input must insure that the extra add-one command arrives either before or between normal count pulses; otherwise it could be missed.

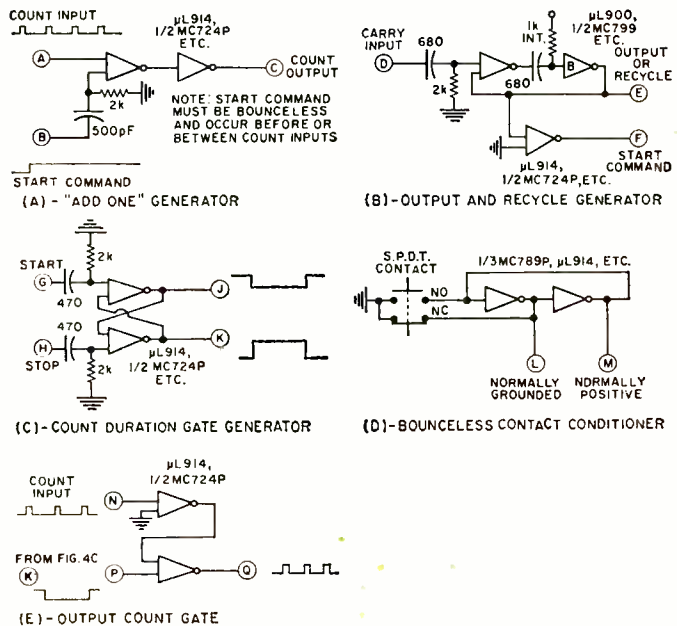
### Control Circuitry

We do have to add some outside circuits to get the counter to work. Even with the most complicated version of these circuits, we still gain a lot in parts count and simplicity, where we swap one set of outside logic for simplicity in six or seven decades.

Let's turn to some control circuit blocks. Fig. 4 shows some RTL versions of these control blocks.

Fig. 4A is an "Add One" circuit. It combines the input count pulses with a single pulse taken from the leading edge of a Start Command rectangular waveform. The leading edge of the Start Command is differentiated and then *or*-ed with the normal input counts. For this circuit to work, we have to guarantee that the Start Command goes positive either before or between the count pulses, and that the Count input line is normally grounded between input counts. (Continued on page 66)

Fig. 4. Some RTL versions of control circuits required when using predetermining counter for applications shown in Fig. 5.



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## Predetermining Decimal Counter

(Continued from page 36)

Fig. 4B is an output and recycle circuit. It takes the positive-going Carry output and converts it to a single high-power pulse of controlled duration, usable either as an output pulse or to reset the counters to 999. An inversion gives us a new Start Command for recycling purposes, if needed.

Fig. 4C is a Set-Reset Start Command flip-flop that gives a signal that lasts for the count period. Fig. 4D is a bounceless push-button or mechanical contact conditioner, needed to prevent noise from erratically triggering the counter. Fig. 4E is a count gate that may be used to route input counts to an output only during the counting time.

### Building Counting Systems

We'll rarely need all of the control blocks at once. Fig. 5 shows some uses for the control circuit blocks.

Fig. 5A is a predetermining process control counter. The first time around, a Reset button is pressed, followed by a Start Command. An a.c.-power-control output is provided for the time it takes to set up the selected count. Reset is automatic on all succeeding counts.

Fig. 5B is a lab scaler or frequency synthesizer that provides one output count for  $n$  input counts, where  $n$  is what you set into the counter. Input and output frequencies or pulse rates will be related by  $1:n$ . Use this for nuclear event counting and lab scaling, as a musician's pitch reference, for a precision audio oscillator or signal generator, or as a v.f.o. replacement.

Fig. 5C shows a precision photo timer that counts the power line for excellent long-term accuracy. Divide-by-six versions of this counter can also be built containing one less IC. Fig. 5D shows a calculator or computer control circuit that has several uses. For keyboard entry, it can generate  $n$  pulses as selected. As part of a rate calculator or computer, it can gate all pulses arriving at input "Y" for a length of time determined by  $n$  of the pulses arriving on input "X." By properly relating X and Y, squares and square roots, multiplication and division, sines and cosines, etc. are easily included with some simple "rate multiplier" circuitry. ▲

Fig. 5. Block diagrams showing some applications for predetermining counter and control circuits. Refer back to Fig. 4.

