How to Build a Memory With One Layer Printed Circuits

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The 2102 static programmable random access memory is a fairly obvious integrated circuit to use for a memory. It is easy to interface to just about any microprocessor or minicomputer. It costs from 0.1 to 0.3 cents a bit, buying from ads in BYTE or from lots of other possible sources.

What's not obvious is how you physically connect a group of eight or more 2102s for a 1 K x 8 or larger memory. We have ten address lines, a write line, an enable line, and two supply runs that have to go in parallel to each and every package. At the same time, separate input and output leads have to be provided in series for each different IC.

One elegant and very compact layout method is to use double sided, plated through boards and leads routed between IC pins. The trouble with this method is that plated through boards are extremely expensive, and there's no reasonable way to manufacture them on your kitchen table. Worse yet, the plating of holes makes removal of soldered parts very difficult, and the close tolerances of routing leads between pins invites trouble from solder splashes. Using double sided boards without plate through holes is even worse, since you have to solder top and bottom, and use of sockets or Molex *Soldercons* gets very ugly, if not downright impossible.

Single sided layouts, of course, are out of the question since they take far too many jumpers. Or do they?

Single Sided Layouts

Here's a simple technique that lets you build virtually any memory you want, using easy home brew low technology single sided boards without routing connections between IC pins, using piggyback ICs, or similar hassles. You can use direct soldering, Soldercons, or sockets per your choice. Whatever method you pick, the ICs are easy to install, test, and replace. The only penalty this method has is that you pay around 50% extra in the way of board area. And believe it or not, all it takes is *six* jumpers. And two of these are for convenience and can be eliminated.

The trick to all this is to pick very carefully what we call a jumper. Figure 1 shows the secret. Four of our "jumpers" are small strips of double sided PC board, 0.2 inch (0.508 cm) high and 5 inch (12.7 cm) long. The foil is somehow selectively removed so that each side touches the edge at only eight places. You can do this by etching, filing, carving, nibbling, scribing, chewing, routing, punching, notching, or just about any way that's convenient. Or, if you don't like using PC material for jumpers, you can use back to back insulated metal strips (Rodgers bus strip style), or you can forget

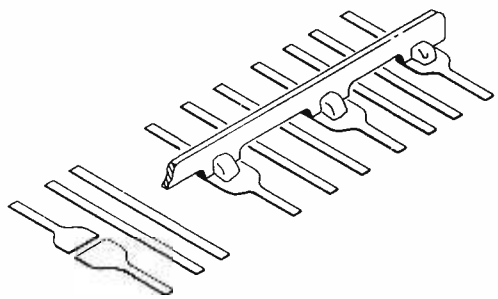


Figure 1: The secret of low cost single sided "no hassle" memory printed circuit layouts is jumper strips made from double sided PC material. Only four such jumper strips are required for the 1 K by 8 memory circuit. Pads on the printed circuit are arranged so that one electrical bus is connected to each side of the jumper strip. Electrical and mechanical connection of bus strips to the printed circuit is accomplished using fillets of solder.

the whole thing and use a Vector wiring pencil or an Applied Solder-Wrapper. What you end up with is one jumper strip that does the job of 14 individual jumpers (seven on each side).

Figure 2 shows us the schematic of a typical 1 K x 8 memory that uses 2102s. We've left it unbuffered for simplicity and low cost. Some background information on the 2102 is found in a separate box accompanying this article.

Our 1:1 PC layout is shown in figure 3, along with the pattern for one side of a typical bus strip jumper. The board has 25 mil (0.64 mm) lines on 25 mil (0.64 mm) centers and no routing between IC pins. With reasonable care, you should be able to handle this on a kitchen table PC lab setup. (I use a kitchen stove myself.) The output pins are conveniently grouped to a separate supply, address, data, and control runs as shown in figure 4. Two jumpers are used to

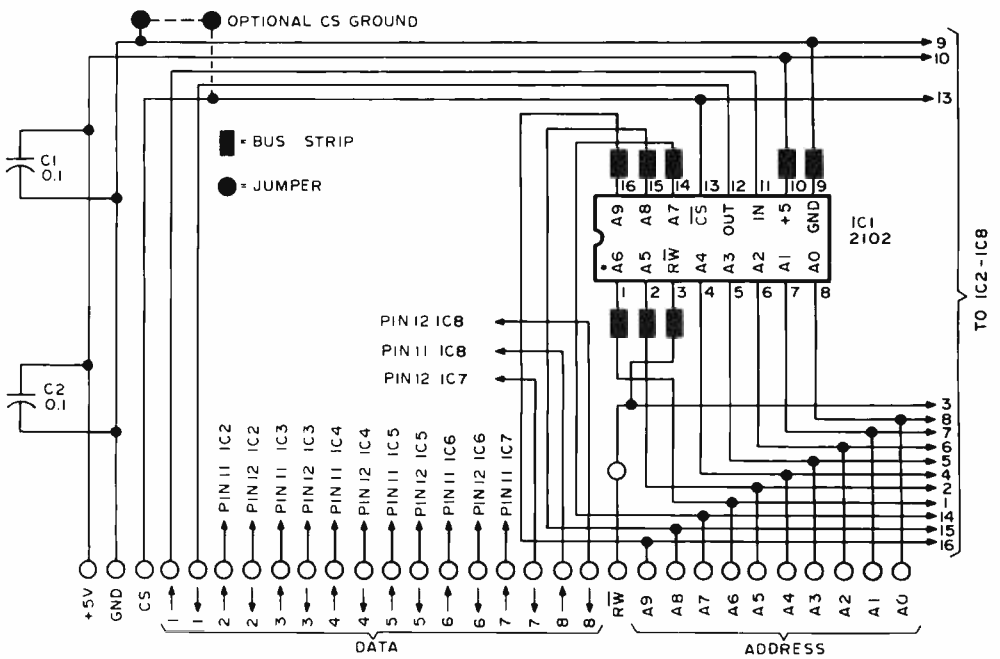


Figure 2: Schematic of a 1 K by 8 Memory Module. This diagram shows one of the eight 2102 memory circuits; IC2 to IC8 are connected in parallel.

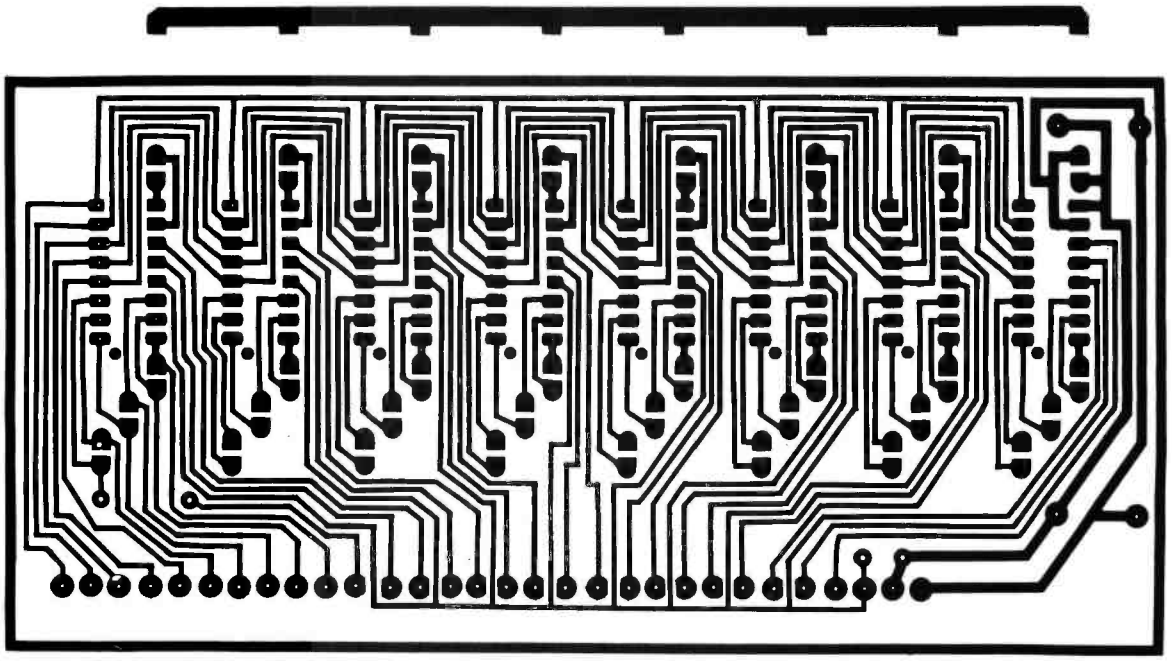


Figure 3: One to one PC Layout Pattern. The 1 K by 8 memory module can be fabricated at home using this pattern. The jumper strip silhouette is shown at the top of the figure. When drilling holes after etching, use the following sizes: #67 drill for the 128 IC pin holes; #60 drill for the four holes used to mount two bypass capacitors from +5 volts to ground; 0.0625 inch (1.5875 mm) drill for the 30 holes used to mount Molex connectors at the edge.

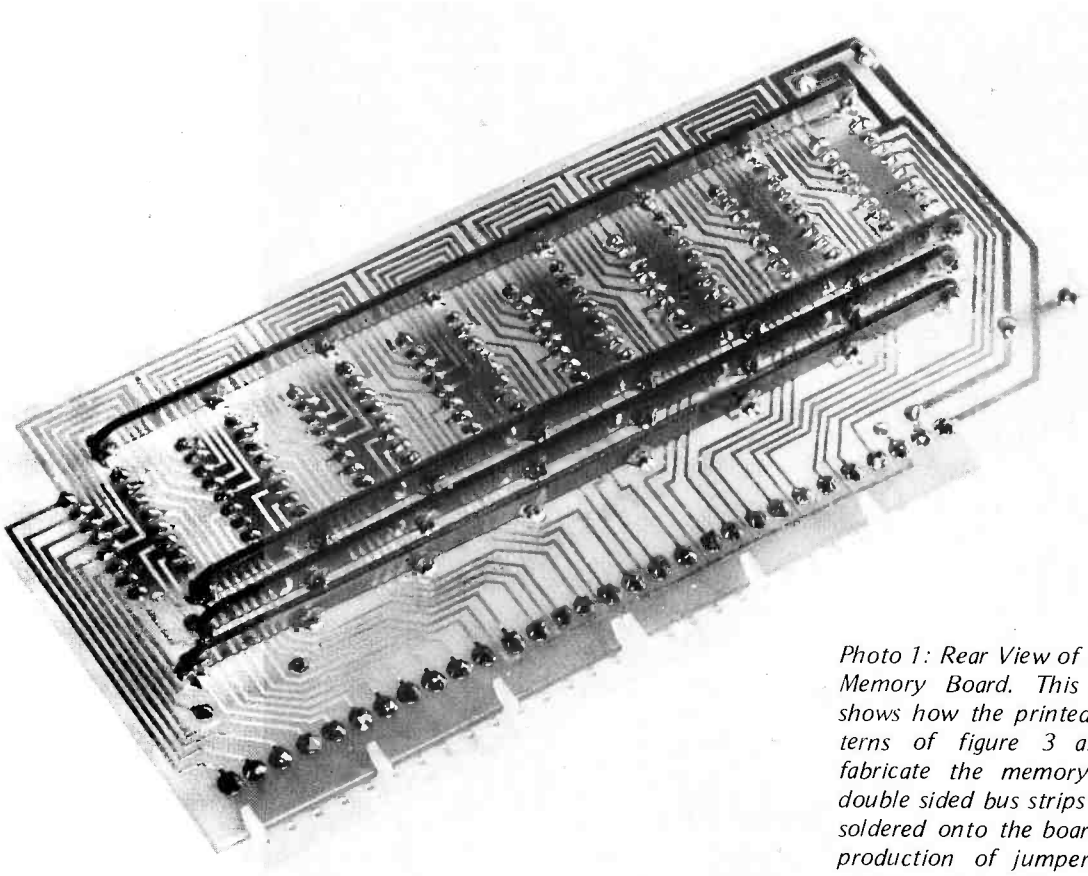


Photo 1: Rear View of the 1 K by 8 Memory Board. This photograph shows how the printed circuit patterns of figure 3 are used to fabricate the memory. The four double sided bus strips required are soldered onto the board. The mass production of jumpers with this method saves time and effort in construction of the board.

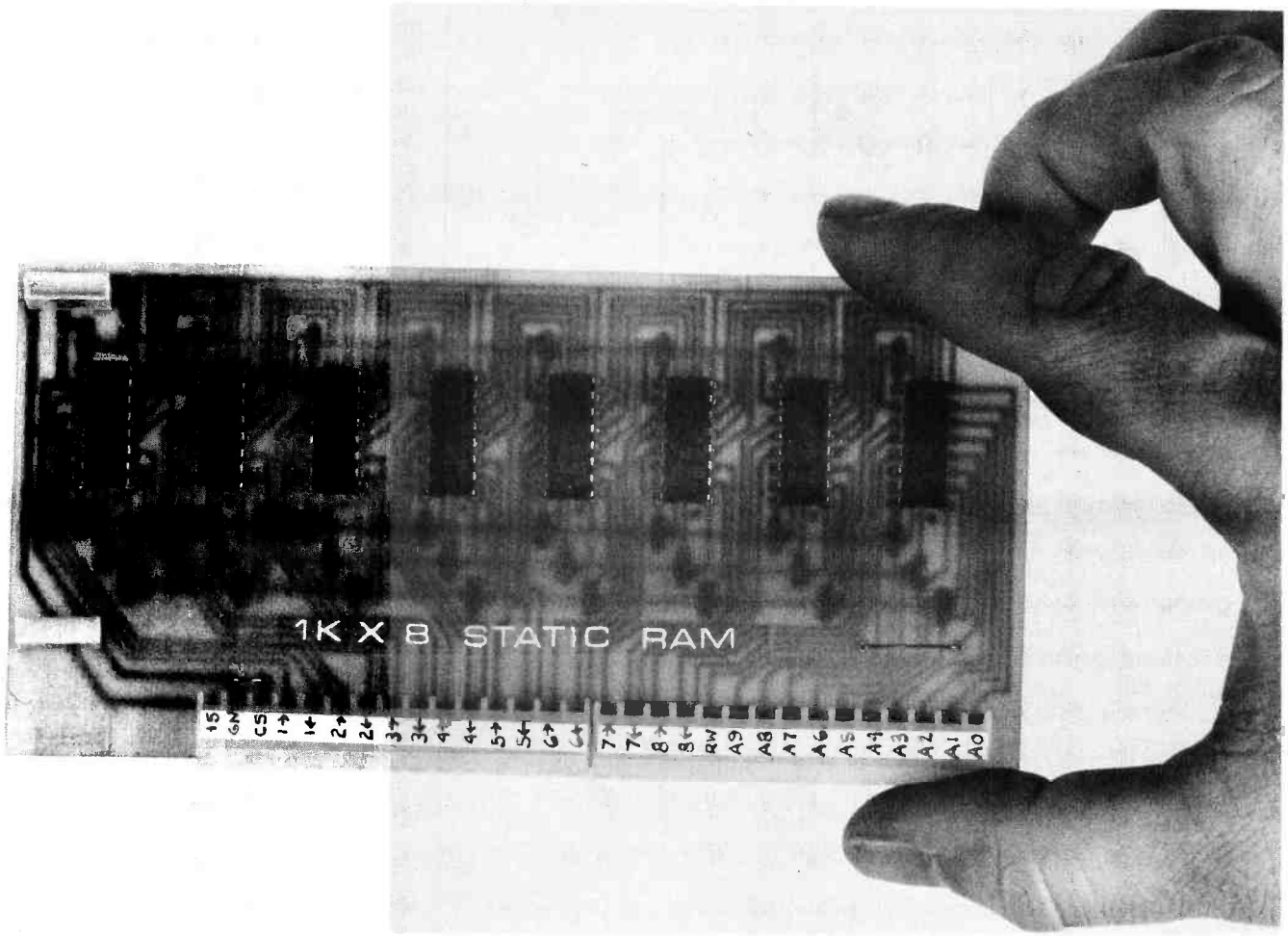


Photo 2: Front View of the 1 K by 8 Memory Board. The Molex edge connectors run along the bottom of the board. In the hand printed notations on the connectors, arrows indicate the direction of data flow for the data pins numbered 1 through 8.

line up the Chip Enable and Write pins in sensible places. Two 0.1 uF capacitors provide supply decoupling.

This particular layout is for 2102s, but you can easily use the same technique for 2101s, 2111s, 2112s, 5101s, dynamic memory, or just about anywhere else you have to connect lots of parallel leads to a bunch of ICs. The edge connector layout has been set up for Molex sockets or socket pins on 0.156 inch (0.396 cm) centers. You can use the sockets at the bottom as shown in photo, or the pins can be set up for a stacked board arrangement according to your needs.

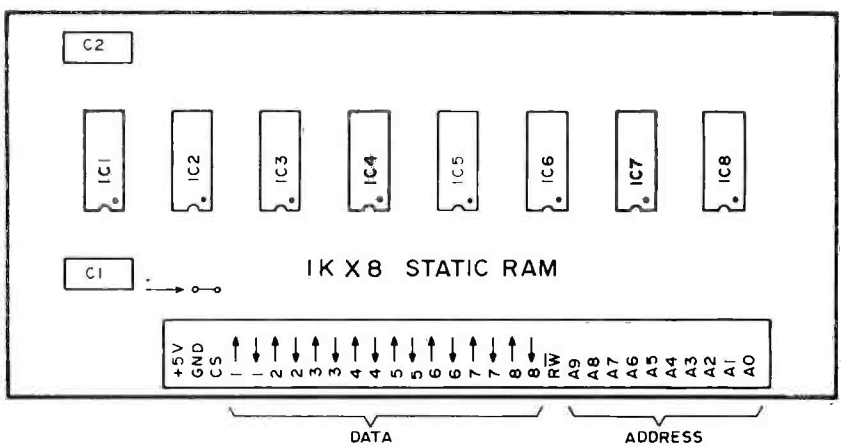
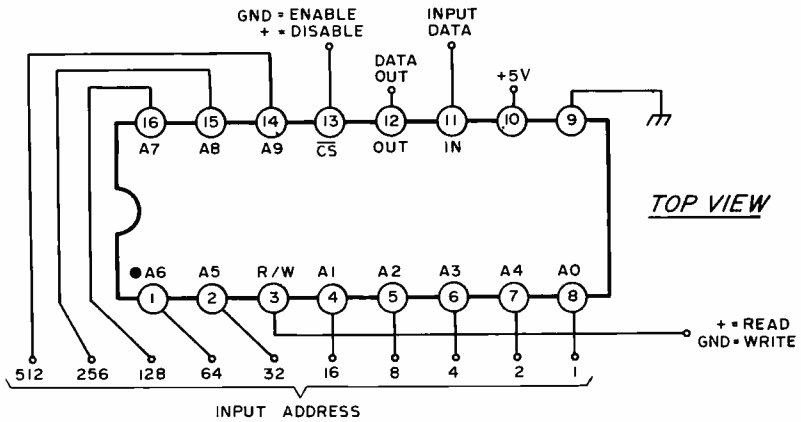


Figure 4: Component Placements. This diagram shows the location of the eight integrated circuits, two power supply bypass capacitors and edge connector pins. The arrow (*) identifies the optional chip select jumper wire.

Using It

The memory will need +5 volts at half an amp (much less if you use premium low power or CMOS RAMs). The ten address lines A0 through A9 select one of the available 1024 words. You can redefine these address lines any way you want. The only thing that's important is that each bit in the word sees the same address at the same time. Our special jumpers have done



STATIC RANDOM ACCESS MEMORY 2102

This is a static random access memory organized 1024 x 1 in a 16 pin package with separate input and output leads. Information may be rapidly read into and non-destructively read out of memory at system speeds. No clocking or refresh is needed. Storage is volatile with data being held only so long as supply power is applied.

To read, pin 13 is given a low level and pin 3 is given a high level. A binary address applied to the ten input address pins will select an internal storage cell and output the data in that cell.

To write, pin 13 is given a low level, and pin 3 is given a high level. A binary address is applied to the ten input address pins to select an internal storage cell. The write input, pin 3, is then brought low and returned high (a "write pulse"). *All address lines must be stable immediately before, during, and immediately after the low state on pin 3.*

All inputs and outputs are TTL and CMOS compatible. The output will drive one TTL load. Making pin 13 positive will float the outputs and ignore write commands. Outputs from separate devices may be connected in parallel so long as only one circuit is enabled at a time.

Access time varies with the manufacturer and the grade of the device. A 800 nanosecond read time and a 400 nanosecond write pulse is typical for a non-premium unit.

Supply power is 70 milliamperes or less, again depending on the grade of the device and the manufacturer.

Note that input addresses may be redefined in any manner convenient for circuit layout. **[Reprinted from Chapter 2 of TVT Cookbook (Sams).]**

this for us already. Data goes in on the eight input lines and out on the eight output lines. The output lines are TTL compatible and drive one standard TTL load. These lines are tristate, so the chip selects can be used to control busing of multiple memory cards.

If you have only one memory card, you can permanently ground the chip select with a jumper. If you have more than one, you have to be sure to ground and enable only one memory card at a time. The tristate memory outputs let you connect many cards in parallel, so long as you enable only one at a time.

The WRITE input should normally be held high. To enter data into memory, briefly bring this input low. The minimum write time depends on the 2102 you're using. Typical minimum times range from 300 to 700 nanoseconds. Check the data sheet for your particular IC.

One very important detail you will want to watch for: Be sure all your address inputs are stable immediately before, during, or after a write pulse. If you try to change addresses while writing, certain internal locations will get "flashed" during the internal decoding, and some unexpected data changes can result.

The 2102 is set up for a separate input and output bus. If you are using a common IO system, you should consider 2101s, 2111s, or 2112s instead. Otherwise, you can add an external bus transceiver such as an AMD 26S10, a TI 75138 or a Motorola 3443. A typical transceiver setup was shown in figure 7, page 17, BYTE No. 3. Note that several cards can share a single bus transceiver so long as you ground only a single chip select at a time. Additional address inputs and a suitable decoder can be used as a card or a page select. ■

BYTE'S BITS

A NEW COMPUTER STORE

One of the latest additions to the ranks of computer retailing and service stores is The Computer Store, 120 Cambridge St, Burlington MA 01803. The store opened in late January, and initially carries the Altair line in addition to numerous related products and services.

A Software Note from Processor Technology: FOCAL™ Language Release

Effective February 15 1976 Processor Technology Corporation released a version of the Digital Equipment Corporation's FOCAL language implemented to run on 8080 based microcomputers. FOCAL, a registered trademark of DEC, is an interactive interpretive language similar to BASIC. Included with the language are high level mathematical functions such as sine and tangent functions.

Cost of a paper tape of the language's object code is $3 and is part of a nationwide dealer promotion package. A source listing is also available as a part of the package, with the conditions of distribution set by the individual dealer.

Processor Technology has also released a resident Assembly Language Operating System, known as Software Package #1, which is available in source form for $3. Contact the factory or your local microcomputer dealer for further details.

Processor Technology is located at 2465 Fourth St, Berkeley CA 94710.